



DESIGN-IN WITH WINBOND W39V040B/W39V080A(LPC) PRODUCT

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1. GENERAL DESCRIPTION

W39V040B/W39V080A LPC flash are application-specific devices which are used for non-Intel Chipset solution. There are three major parts listed in this comparison notice to identify the differences among Winbond 4M/8M LPC and the equivalent parts of SST, STM.

2. DETAIL DESCRIPTION

The comparison on Function, Command, and Pin Assignment in Programmer Mode and LPC mode is described in the following:

2.1 Function

4M/8M LPC Flash Compare Table

FUNCTION COMPARISON	WINBOND W39V040B W39V080A	SST 49LF004B W49LF080A	STM M50FLW040A/B M50FLW080A/B
Sector Definition	64Kx8	Diversified 4K/64K	64Kx8
Command Sets	AMD-LIKE command	AMD-LIKE command	INTEL-LIKE command
LPC BUS(LPC) Interface Mode	LPC	LPC	FWH and LPC
Programmer Interface Mode	Yes	Yes	Yes
Random Number Generator	No	No	No
Internal Boot Block Lockout	Yes	Yes	Yes
External H/W Protect Pins	Yes	Yes	Yes
Chip Erase	No	Yes	No
R/W Lock Registers	Yes	Yes	Yes
Multiple Device Selection	Yes	Yes	Yes
Device ID Register	Yes	Yes	Yes
Vpp For Fast Programming	Yes	No	Yes
Erase/Program Suspend	No	No	Yes
General Purpose Inputs Register	Yes	Yes	Yes

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2.2 Command

Please note that the STM M50FLW040 /M50FLW080 belong to its respective command system and it is different from Winbond and SST command system. Therefore, the following table is based on each vendor defined command definitions.

FUNCTION COMPARISON	WINBOND W39V040B W39V080A	SST 49LF004B 49LF080A	STM M50FLW040A/B M50FLW080A/B
Byte Program	A0H	A0H	40H or 10H
Sector Erase (SST Block)	30H	50H	D0H
Product ID Entry	90H	90H	90H
Product ID Exit	F0H	F0H	FFH
Block Erase/Program Suspend	----	----	B0H
Block Erase/Program Resume	----	----	D0H

2.3 Pin Assignment

The W39V040B and W39V080A used for PC (NB) system with non-Intel chipset solution. Its pin assignment is arranged to be easily adapt to each non-Intel system. Therefore, all minor differences between Winbond and other vendors can be ignored.

2.3.1 In Programmer Mode

Table 1. 32L-PLCC Pin Assignment in Programmer Mode

SST 49LF004B 49LF080A	STM M50FLW040 M50FLW080	WINBOND W39V040B W39V080A	PIN ASSIGNMENT IN PROGRAMMER MODE	WINBOND W39V040B W39V080A	STM M50FLW040 M50FLW080	SST 49LF004B 49LF080A
---	VPP	Vpp	1	32	VDD	VDD
RESET#	RESET#	RESET#	2	31	R/C#	R/C#
A9	A9	A9	3	30	A10	A10
A8	A8	A8	4	29	IC	IC
A7	A7	A7	5	28	GND	GND
A6	A6	A6	6	27	---	---
A5	A5	A5	7	26	---	GND
A4	A4	A4	8	25	VDD	VDD
A3	A3	A3	9	24	OE#	OE#
A2	A2	A2	10	23	WE#	WE#
A1	A1	A1	11	22	RY/BY#	RY/BY#
A0	A0	A0	12	21	DQ7	DQ7
DQ0	DQ0	DQ0	13	20	DQ6	DQ6
DQ1	DQ1	DQ1	14	19	DQ5	DQ5
DQ2	DQ2	DQ2	15	18	DQ4	DQ4
GND	GND	GND	16	17	DQ3	DQ3

Note: (---: NC)

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2.3.2 In LPC Mode

Table 2. 32L-PLCC Pin Assignment in LPC Mode

SST 49LF004B 49LF080A	STM M50FLW040 M50FLW080	WINBOND W39V040B W39V080A	PIN ASSIGNMENT IN LPC MODE		WINBOND W39V040B W39V080A	STM M50FLW040 M50FLW080	SST 49LF004B 49LF080A
---	VPP	VPP	1	WINBOND 32-LEAD PLCC STANDARD PINOUT	32	VDD	VDD
RESET#	RESET#	RESET#	2		31	CLK	CLK
FGPI3	FGPI3	FGPI3	3		30	FPGI4	FPGI4
FGPI2	FGPI2	FGPI2	4		29	IC	IC
FGPI1	FGPI1	FGPI1	5		28	GND	---
FGPI0	FGPI0	FGPI0	6		27	---	---
WP#	WP#	WP#	7		26	---	GND
TBL#	TBL#	TBL#	8		25	VDD	VDD
ID3	ID3	ID3	9		24	INIT#	INIT#
ID2	ID2	ID2	10		23	#LFRAME	#LFRAME
ID1	ID1	ID1	11		22	---	---
ID0	ID0	ID0	12		21	---	---
LAD0	LAD0	LAD0	13		20	---	---
LAD1	LAD1	LAD1	14		19	---	---
LAD2	LAD2	LAD2	15		18	---	---
GND	GND	GND	16		17	LAD3	LAD3

Note: Different pin assignment has been highlighted in bold font.

2.4 Sector Erase Interval

System designer can use DQ6(Toggle Bit) or DQ7(Data Polling bit) to determine whether a erase operation is complete or in progress.

While doing end-check of sector erase, please note the followings:
The minimum interval between toggling-check (or polling-check) should be more than 50ms. Only sector erase needs such special care and this rule is suitable for both W39V040B and W39V080A.

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2.5 Toggle Bit Algorithm For Sector Erase Only

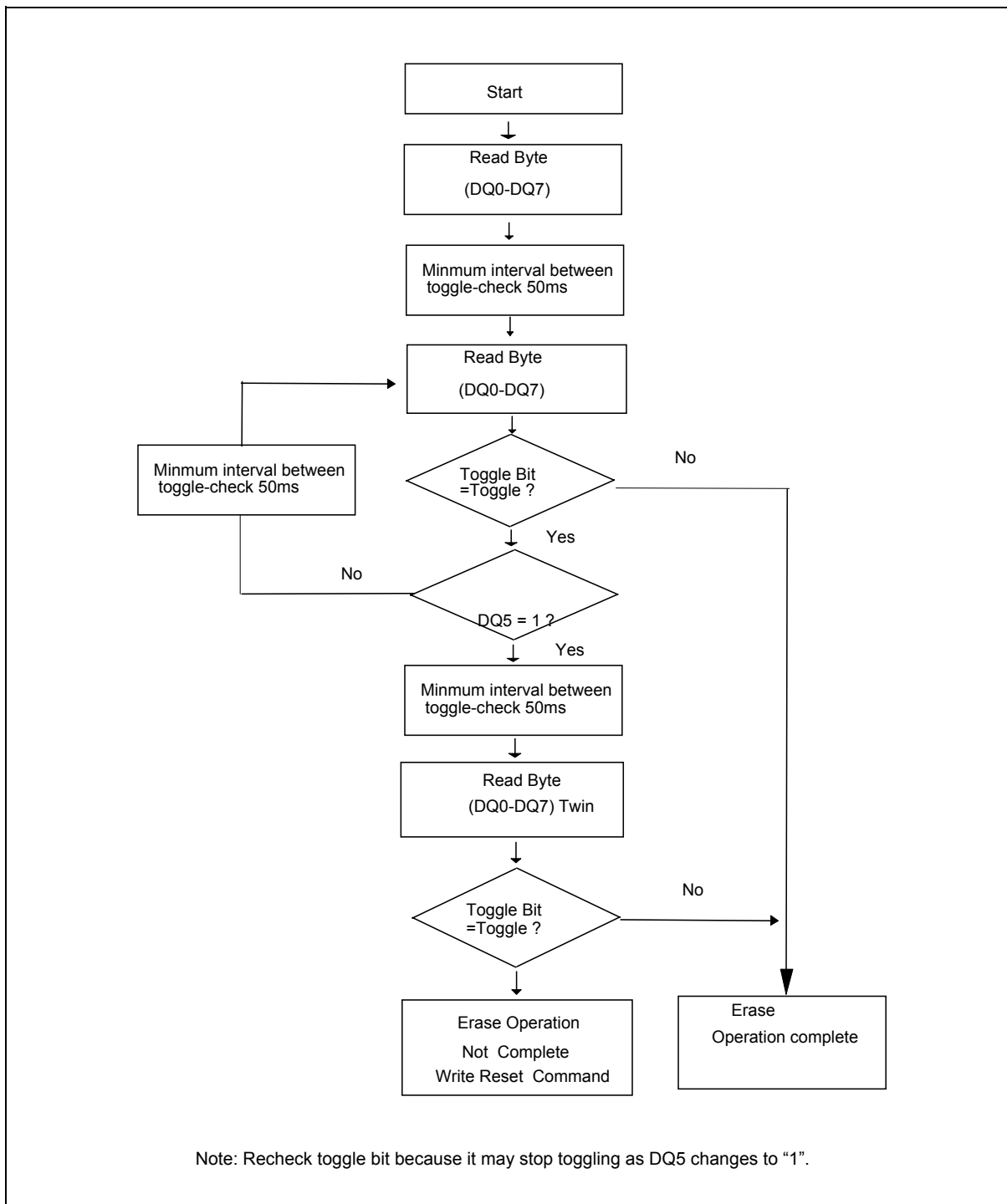


Figure 1

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3. CONCLUSION

The W39V040B and W39V080A are well supported by all famous third parties like BIOS vendors AMI, Award/Phoenix, and Programmer vendors (please refer to our support list.) They have made efforts to cover the difference on device's command sets and programming algorithm. Therefore, there is no compatible issue for users to directly use it in their system.

4. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Nov. 26, 2004	-	Initial Issued



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