



#RESET, V_{PP} ELECTRIC POTENTIAL SWITCHING CIRCUIT FOR W28XXX SERIES FLASH

1. GENERAL DESCRIPTION

If the flash memory is used for the system startup, the flash memory should be reset to read array mode at power-up. When the read array mode has been changed into the status register read mode, a system program cannot be called correctly and the system cannot operate correctly. Moreover, at the worst, any data written into flash memory may be rewritten. In general, this may happen due to the system circuit structure, wiring pattern of printed board, or operating environment. Otherwise because of any noise such as control signal pulse noise upon an operation and power supply noise.

In order to avoid those unforeseen circumstances, this application note describes (1) how to supply the power and (2) how to prevent an operation error by controlling the #RESET pin and V_{PP} pin.

2. HOW TO PREVENT OPERATION ERROR BY CONTROLLING #RESET PIN

#RESET Pin

The #RESET pin not only reduces the power consumption of device to a negligible level (Reset mode) but also functions as a device reset input. Using this function, flash memory can be protected against an operation error due to the power supply noise at power-up or the control signal noise.

Preventing operation error made due to command mis-recognition

After turning on the power supply or resetting by the #RESET pin, the flash memory usually enters a read array mode. However, unforeseen erasing/writing is done by the mis-recognition of command, in general, due to noise at power-up, noise of control signal (#CE, #WE, etc.) or system noise when the #RESET pin changes from "low" to "high". Moreover, due to such mis-recognition, a read array mode is replaced with a status register read mode. As a result, any programs necessary for system start cannot be read and the system may not start correctly (Figure 1). t_{PHL} is a recovery time (#RESET "high" recovery to #CE going low time). Refer to the description of "AC Characteristics - #CE Controlled Writes" of the specifications.

Otherwise the flash memory is initialized by writing the Read Array (FFH) command three times or more after turning on the power supply or changing the #RESET terminal status from "low" to "high". The status register read mode can be returned to the read array mode (Table 1), the inadvertent rewriting due to the command mis-recognition can be prevented. The Read Array (FFH) command is written three times or more for the purpose of supporting a three-cycle command.

#RESET, V_{PP} ELECTRIC POTENTIAL SWITCHING CIRCUIT FOR W28XXX SERIES FLASH

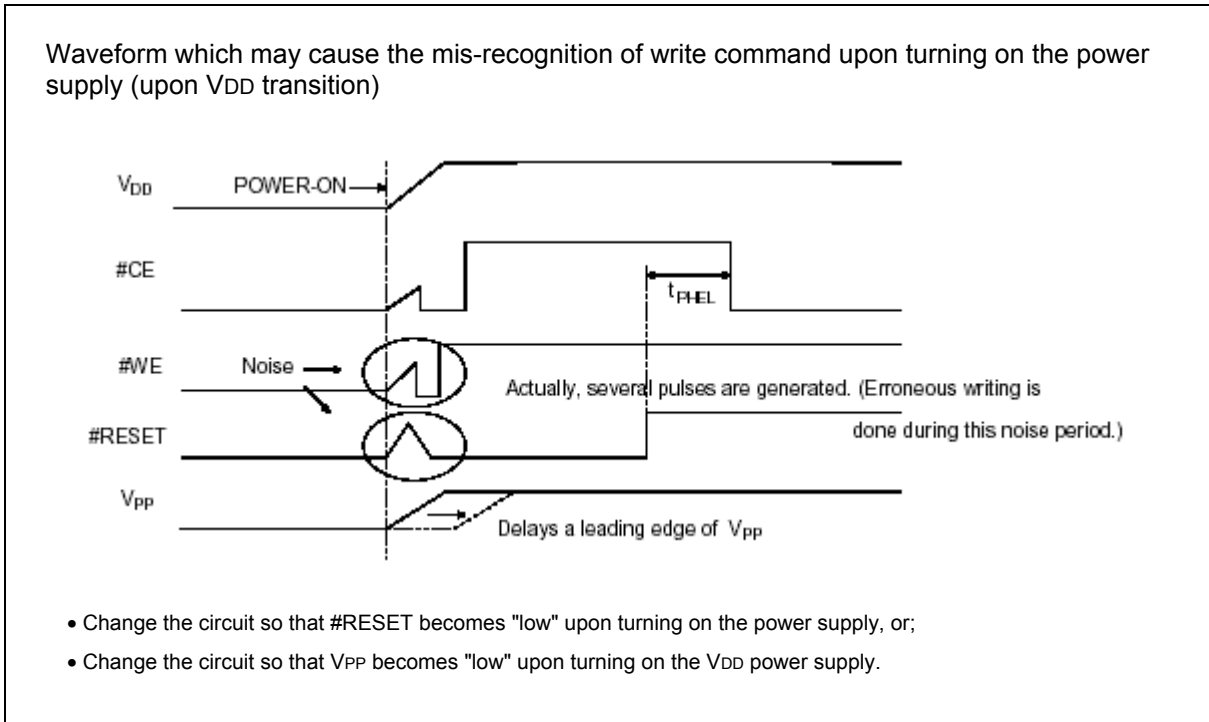


Figure 1. Example of noise upon turning on power supply or upon fluctuation of #RESET signal

Table 1. How to initialize upon turning on power supply or upon fluctuation of #RESET signal

<p>(1) Turning ON the power supply - Writing FFH three times or more</p> <p>(2) Setting the #RESET pin from "low" to "high" - Writing FFH three times or more</p>

Preventing operation error made due to power supply noise such as unforeseen power failure

By setting the #RESET pin to "low", the Reset mode is enabled and the device is reset (initialized). That is, when the #RESET pin is set to "low", all the active operations are terminated and the device is initialized. This function is useful to prevent unforeseen rewriting due to glitch noise upon turning on the power supply or due to the considerable power supply voltage drop.

After the #RESET pin has become "low" during writing/erasing and the device has been initialized, even if the #RESET pin returns to "high", the writing/erasing is not restarted. Therefore, a write/ erase command must be issued again.

Example of control circuit of #RESET pin

If the system contains a reset control circuit, the #RESET pin can be controlled through a system-reset line. The #RESET pin must be kept in a low level (V_L) until approximately 100ns at least has passed after the power supply V_{DD} has been in a recommended operating voltage range. Figure 3 shows an example of reset circuit.

#RESET, V_{PP} ELECTRIC POTENTIAL SWITCHING CIRCUIT FOR W28XXX SERIES FLASH



The flash memory enters the read array mode after the #RESET pin has changed from "low" to "high". Then, to read the correct array data, you must wait for a period of t_{PHQV} specified in any applicable specifications. Therefore, a CPU reset input may have to be equipped with an RC delay circuit so that the flash memory can be read before the CPU issues a memory read cycle. It depends on the number of clock cycles from the completion of CPU reset to the first flash code fetch whether the RC delay circuit is necessary or not. Some flash memories may specify t_{PLRH} (Note 2), in addition to t_{PHQV} (Note 1). For the details, refer to the specifications (the description of "Reset Operation").

Note 1: t_{PHQV} is an output delay time (#RESET "high"). Refer to the description of "AC Characteristics - Read Operation" of the specifications.

Note 2: t_{PLRH} is the #RESET "low"-R_Y/#B_Y "high" time. Refer to the description of "Reset Operation" of the specifications.

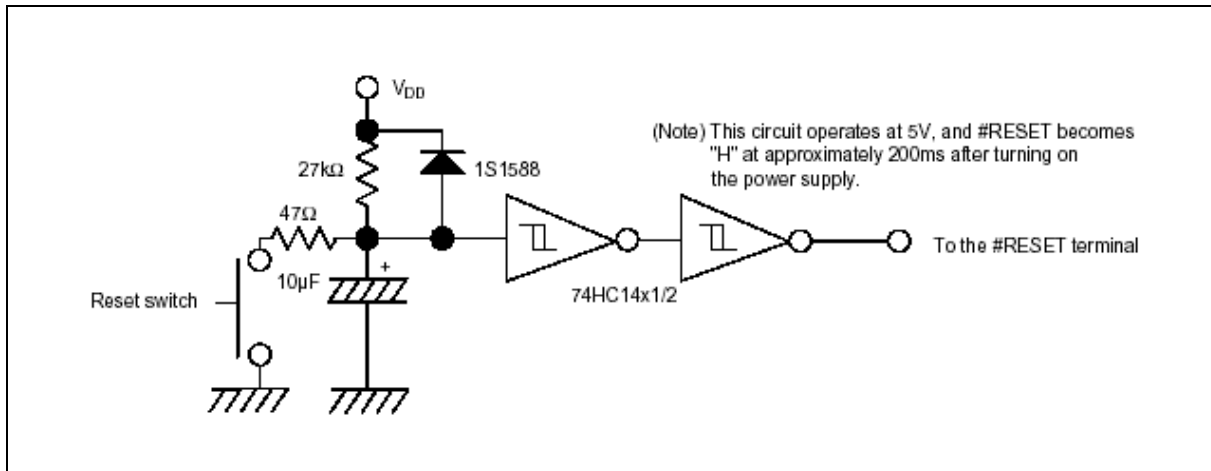


Figure 2. Example of reset circuit

3. HOW TO PREVENT OPERATION ERROR BY CONTROLLING V_{PP} PIN

V_{PP} Pin

Writing/erasing operation is disabled if the V_{PP} is the V_{SS}.

Taking into consideration the case shown in Figure 1 and data protection at power-up, it is recommended to apply the specified voltage on the V_{PP} after the V_{DD} power supply voltage has become stable.

Example of control method for V_{PP} pin

To prevent the unwanted writes, apply 0V on V_{PP} upon power-up and during read operations, and apply the specified voltage on V_{PP} during write or erase operations. Then, data in flash memory can be protected. Figure 3 and Figure 4 show the control methods for V_{PP} pin via GPIO (General Purpose Input/Output) line. Figure 3 shows the control method for flash memory of which V_{PP} is used for power supply pin. Figure 4 shows the control method for flash memory of which V_{PP} is used for logic input.

Write and erase operations are disabled if the V_{PP} is set to the V_{SS}. The specified voltage on V_{PP} for reliable write and erase operations is described in the device specifications or data sheet. If any over-

#RESET, V_{PP} ELECTRIC POTENTIAL SWITCHING CIRCUIT FOR W28XXX SERIES FLASH



voltage or negative voltage is applied to the V_{PP} pin, the device may be damaged or device reliability may be affected. Be sure to follow the voltage range described in the device specifications.

In general, a maximum electric current is generated upon writing or erasing. If writing or erasing is executed in several devices simultaneously, a consumption current increases in proportion to the number of such devices. Take care not to generate any fall of electric potential and any noise in the V_{PP}.

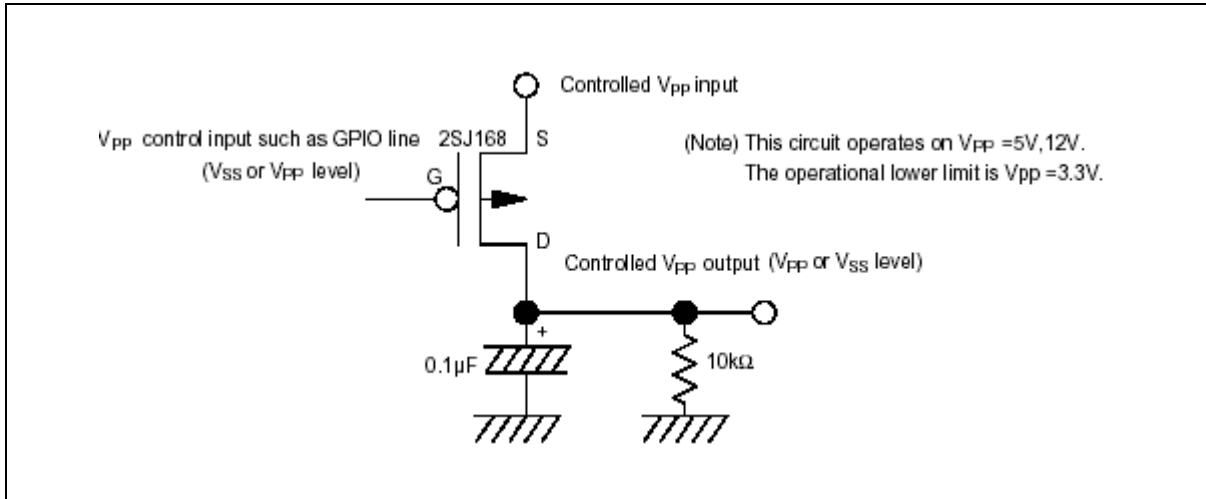


Figure 3. Example of control method for V_{PP} power supply

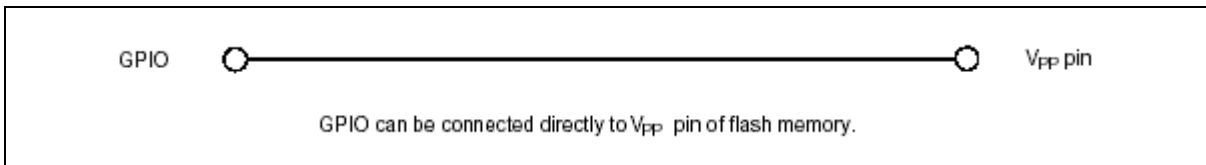


Figure 4. Example of control method for V_{PP} logic input

4. NOTES ON WIRING OF V_{DD}/V_{PP} PIN

Decoupling of Power Supply

Upon designing any system, the system circuit designer should pay attention to the under-mentioned three power supply currents:

- Standby current (ICCS)
- Operating current (ICCR)
- Peak value of transient current flowing upon a rising edge and falling edge of the #CE signal or #OE signal.

The intensity of transient current depends on the capacitive load and inductive load of device output. The power supply noise due to transient current can be suppressed by locating any decoupling capacitor of suitable capacity at an appropriate position. Connect a 0.1 µF ceramic capacitor between flash memory V_{DD} and V_{SS} and between V_{PP} and V_{SS} (only when V_{PP} is used as power supply). The ceramic capacitor should be located as close as possible to a flash memory package pin. Additionally

#RESET, V_{PP} ELECTRIC POTENTIAL SWITCHING CIRCUIT FOR W28XXX SERIES FLASH



for every eight devices, a 4.7 μ F electrolytic capacitor should be connected between VDD and VSS at the array's power supply connection. In the event that less than eight flash memory components are used a single 4.7 μ F bypass capacitor is still necessary. Those capacitors can suppress the voltage drop arisen from the inductive load due to a pattern on a printed board. 4.2 Pattern on printed board Upon designing any printed board equipped with flash memory, the system circuit designer should pay attention to the wiring pattern of VDD and VPP (only when VPP is used as power supply). In order to suppress any spike noise and overshoot of VDD and VPP voltage (only when VPP is used as power supply), make the power supply wiring pattern as wide as possible and as short as possible.

5. CONCLUSION

By setting the #RESET pin to a low level, the Reset mode is enabled. This mode reduces the power consumption of device to a negligible level and, moreover, the device is initialized. This function is useful to protect any data against unforeseen writing/erasing especially not only when the power supply glitch noise has been generated but also when the system power supply voltage has dropped beyond an allowable operating limit.

However, to read the correct array data after the #RESET pin has changed from "low" to "high", you must wait for a period of tPHQV specified in any applicable specifications. Some flash memories may specify tPLRH, in addition to tPHQV. For the details, refer to the specifications (the description of "Reset Operation").

To prevent the unwanted writes, apply 0V on VPP upon power-up and during read operations, and apply the specified voltage on VPP during write or erase operations. This method can provide the hardware data protection.



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