



DATA PROTECTION METHOD OF W28XXX SERIES FLASH

1. GENERAL DESCRIPTION

The unforeseen rewriting may be executed or a status register read mode may be enabled by recognizing a noise signal as any command by mistake. In general, these may happen, mainly due to the system circuit structure equipped with flash memory, wiring pattern of printed board, operating environment or any noise beyond the specification value upon an operation. Otherwise, because of any input level noise beyond the specification value to the VPP terminal, #RESET signal, #CE signal and #WE signal upon turning on/off the power supply.

If the flash memory is used for system startup, the flash memory should be reset to read array mode at power-up. When the status register read mode has been enabled instead of a read array mode at power-up, due to the above-mentioned noise. The system may not be started up correctly because any programs necessary for startup of the system cannot be read nor executed.

To protect any data against inadvertent rewriting under such situation, it is advisable to protect the data by using the under-mentioned functions upon the system design. For example, when the device power-up, holding the #RESET-"low" is required after the power supply VDD has been in predefined range and also has been in stable there.

2. DATA PROTECTION METHOD OF FLASH MEMORY

The Winbond flash memory has a data protection function. Any data in flash memory can be protected by using the following method.

Data protection in boot block flash memory

Table 1 lists the Winbond boot block type flash memories. By setting the #WP pin to "low", an erasing and writing to a boot block (4K-words x 2) are disabled and the boot block data can be protected. In order to protect data in all the blocks including the boot block, suppress the VPP terminal to the VSS voltage. (Refer to How to protect data with VPP control section)

By setting the #WP pin to "high", erasing and writing to all the blocks including the boot block are enabled.

The 8M/16M/32M has the block lock and permanent lock functions. The block lock-bits gate the write and erase operations. By setting the block lock bit, the erasing and writing into the block are disabled and the data of the block are protected. By clearing block lock-bits, the erasing and writing to blocks are enabled.

Table 1. Boot block type flash memory

BOOT BLOCK MODEL NO.	CAPACITY	BIT	#WP PIN	BLOCK LOCK FUNCTION BY #WP PIN	BLOCK LOCK FUNCTION	PERMANENT LOCK FUNCTION
W28V400	4M	x8/x16	Available	Only Boot Block	N/A	N/A
W28J800	8M	x8/x16	Available	Only Boot Block	Individual block	Available
W28J160	16M	x8/x16	Available	Only Boot Block	Individual block	Available
W28J161	16M	x16	Available	Only Boot Block	Individual block	Available
W28J320	32M	x8/x16	Available	Only Boot Block	Individual block	Available
W28J321	32M	x16	Available	Only Boot Block	Individual block	Available

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3. HOW TO PROTECT DATA OF EACH BLOCK

Using #WP Pin

In the flash memory in which a #WP pin lock command is available, data is protected as follows:

- By setting the #WP pin to "high" in order to set a lock bit of any block and then setting the #WP pin to "low", rewriting in that block becomes unavailable. This allows, for example, to define a locked area in flash memory and unlocked area as a program area and data area respectively.
- In order not to rewrite data, after the particular blocks are locked and then #WP is connected to the Vss. Unless setting the #WP pin to "high", the block lock bits cannot be changed.
- By controlling the #WP pin from "low" to "high", a lock block can be also switched through software.

Using Permanent Lock Command

In the flash memory in which a permanent lock command is available, data is protected as follows:

- In case of 8M/16M/32M, after setting the lock bit of any block, and issuing a permanent lock command, then, erasing/writing in that block becomes unavailable. This allows, for example, to define a locked area in flash memory and unlocked area as a program area and data area respectively.
- By issuing a permanent lock command, an error in setting/resetting the lock bits can be prevented. However, if the permanent lock bit is set once, such permanent lock bit cannot be cleared.
- When the permanent lock bit has been set, even if the #RESET pin is set to VHH, any lock bits cannot be set nor cleared.

4. HOW TO PROTECT DATA WITH VPP CONTROL

If the VPP voltage becomes the VSS electric potential, any data in flash memory cannot be rewritten. Therefore, any unforeseen rewriting does not happen even if a noise signal is mistaken for any command.

Set the VPP voltage to the VSS electric potential if no data is rewritten (read only memory). By configuring the system so that the VPP voltage is switched to a recommended operating voltage only upon the erasing/writing a data. The data can be protected through the VPP control.

5. HOW TO PROTECT DATA WITH #RESET

- By setting the #RESET pin to "low", the flash memory enters the "Reset" mode and erasing/writing in all the blocks becomes unavailable.
- By setting the #RESET pin to "low" in order to protect any data upon the transition of power supply voltage, the flash memory is disabled and the erasing/writing in all the blocks becomes unavailable.
- However, due to the system noise when the #RESET pin has changed from "low" to "high", an unforeseen erasing/writing or the status register read mode may be invoked by the mis-recognition of command.

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6. HOW TO PROTECT DATA WITH #WE CONTROL

To protect a data in flash memory against unforeseen writing/erasing, the OR logic gate and GPIO signal can be combined with the #WE signal, as shown in Figure 1. Then, to reduce the noise on wiring of printed board, wire the output of OR logic gate and the input of #WE terminal of flash memory, which are shown in Figure 1, near to the flash memory package. The GPIO signal is initialized to "high" upon turning on the system power supply and the software controls the GPIO signal so that it becomes "low" upon writing/erasing to flash memory. If the GPIO signal status is always "high", writing/erasing to flash memory is not executed and the flash memory becomes ROM (read only memory).

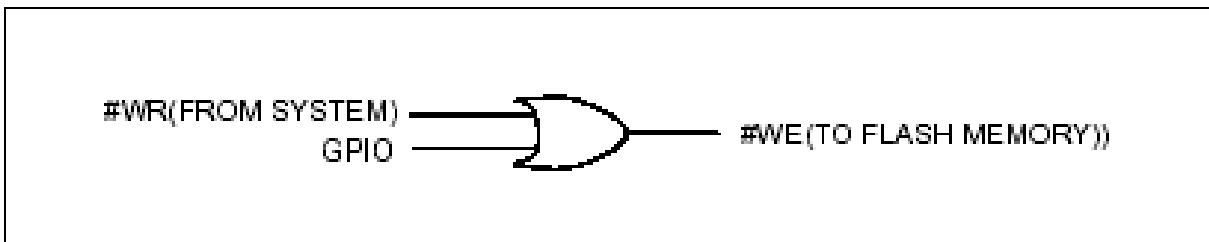


Figure 1. #WE Gating

7. NOTES ON SYSTEM POWER-ON/OFF AND ON RESET WITH #RESET SIGNAL

To prevent an inadvertent writing upon turning on/off the system power supply, the Winbond flash memory disables any writing/erasing under "VLKO" voltage (also called the lock-out voltage, prescribed by the specifications). If the system power supply $V_{DD} \leq VLKO$, the flash memory does not accept any write/erase command. And also, even if the system power supply V_{DD} is VLKO or more, the flash memory does not execute any write/erase operations when the V_{PP} voltage is the V_{SS} voltage or V_{PPLK} voltage or less.

If the system power supply V_{DD} gets less than the "VLKO" voltage during the execution of writing/erasing, such writing/erasing is terminated. Even if the system power supply V_{DD} returns to a recommended operating voltage range after that, writing/erasing is not resumed. Therefore, a writing/erasing command must be issued again.

Due to the power supply noise at power-up or the system noise when the #RESET pin has changed from "low" to "high", an unforeseen erase/write mode or status register read mode may be invoked by the mis-recognition of command (Figure 2). By writing the READ ARRAY (FFH) command three times or more in order to initialize a device after turning on the power supply or changing #RESET from "low" to "high", unforeseen rewriting due to mis-recognition of command can be prevented. Or you can return to the array data read mode from the status register read mode (Table 2). The READ ARRAY (FFH) command needs to be issued three times or more.

DATA PROTECTION METHOD OF W28XXX SERIES FLASH

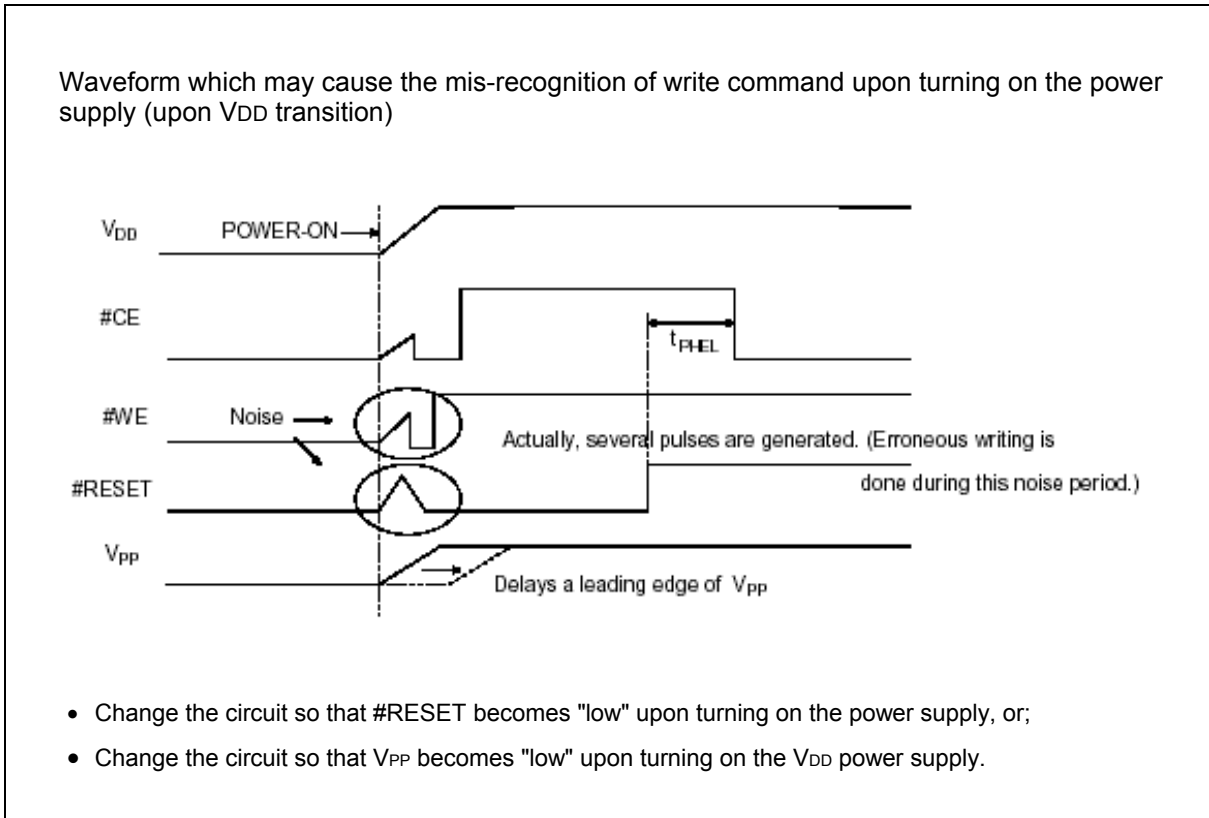


Figure 2. Example of noise upon turning on power supply or upon fluctuation of #RESET signal

Table 2. How to initialize upon turning on power supply or upon fluctuation of #RESET signal

(1) Turning ON the power supply → Writing FFH three times or more
(2) Setting the #RESET pin from "low " to "high" → Writing FFH three times or more

8. CONCLUSION

Due to the system noise or any noise upon turning on/off the power supply, an unforeseen rewriting may be executed or the status register read mode may be invoked by the mis-recognition of command.

In the system design with the Winbond flash memory, more flexible and more excellent data protection circuit can be designed by using hardware write-protection with V_{PP} control, #RESET control and #WP control and software write-protection together.

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